IN THE CLAIMS:

1. (Currently Amended) A computer-readable medium having stored thereon a plurality of instructions, the plurality of instructions including instructions that when executed by a processor cause the processor to implement a ~~computer-implemented~~ system for automatically generating a hierarchical register consolidation structure, comprising:

a graph generator that parses a High-level Design Language (HDL) file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers of external devices identified by said HDL file;

a graph converter, associated with said graph generator, that selectively adds virtual elements and nodes to said intermediate graph to transform said intermediate graph into a mathematical tree; and

a description generator, associated with said graph converter, that employs said mathematical tree to generate a static tree description to form a hierarchical register consolidation structure to provide a logical representation of said microprocessor-accessible registers, node interrelationships, summary bits and masks of said external devices in a programming language suitable for use by a device-independent condition management structure.

2. (Original) The system as recited in Claim 1 wherein said intermediate graph further contains bit offsets associated with said alarm registers.

3. (Original) The system as recited in Claim 1 wherein said description generator further generates an HTML traversable tree representation based on said mathematical tree.

4. (Original) The system as recited in Claim 1 wherein said programming language is C.

5. (Original) The system as recited in Claim 1 wherein said HDL file is produced by a hardware description tool.

6. (Currently Amended) The system as recited in Claim 3 ~~1~~ wherein said condition management structure manages interrupts associated with said external devices employing said static tree or said HTML traversable tree ~~interacts only with a logical representation of said microprocessor-accessible registers, node interrelationships, summary bits and masks~~.

7. (Currently Amended) The system as recited in Claim 1 wherein said graph generator parses said HDL file in three different passes to generate said intermediate graph ~~, said graph converter and said description generator are embodied in sequences of instructions executable in a general purpose computing system~~.

8. (Original) A method of automatically generating a hierarchical register consolidation structure, comprising:

parsing a High-level Design Language (HDL) file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers;

selectively adding virtual elements and nodes to said intermediate graph to transform said intermediate graph into a mathematical tree; and

employing said mathematical tree to generate a static tree description in a programming language suitable for use by a device-independent condition management structure.

9. (Original) The method as recited in Claim 8 wherein said intermediate graph further contains bit offsets associated with said alarm registers.

10. (Original) The method as recited in Claim 8 further comprising employing said static tree description to generate an HTML traversable tree representation based on said mathematical tree.

11. (Original) The method as recited in Claim 8 wherein said programming language is C.

12. (Original) The method as recited in Claim 8 further comprising producing said HDL file with a hardware description tool.

13. (Original) The method as recited in Claim 8 wherein said condition management structure interacts only with a logical representation of said microprocessor-accessible registers, node interrelationships, summary bits and masks.

14. (Original) The method as recited in Claim 8 wherein said parsing, selectively adding and employing are carried out by sequences of instructions executable in a general purpose computing system.

15. (Currently Amended) A computer-readable medium having stored thereon a plurality of instructions, the plurality of instructions including instructions that when executed by a processor cause the processor to implement a ~~computer-implemented~~ system for automatically generating a hierarchical register consolidation structure, comprising:

a graph generator that parses a Verilog hardware description language ~~High-level Design Language~~ (HDL) file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits, bit offsets and masks associated with alarm registers of external devices identified by said Verilog HDL file;

a graph converter, associated with said graph generator, that selectively adds virtual elements and nodes to said intermediate graph to transform said intermediate graph into a mathematical tree; and

a description generator, associated with said graph converter, that employs said mathematical tree to generate a static tree description in a programming language suitable for use by a device-independent condition management structure and an HTML traversable tree representation based on said mathematical tree, wherein both of said static tree description and said HTML traversable tree provide a logical representation of said microprocessor-accessible registers, node interrelationships, summary bits and masks of said external devices.

16. (Original) The system as recited in Claim 15 wherein said programming language is C.

17. (Currently Amended) The system as recited in Claim 15 wherein said Verilog HDL file is produced by a hardware description tool.

18. (Currently Amended) The system as recited in Claim 15 wherein said condition management structure interacts only with said ~~a~~ logical representation of said static tree description or said HTML traversable tree to manage interrupts from said external devices ~~microprocessor-accessible registers, node interrelationships, summary bits and masks~~.

19. (Original) The system as recited in Claim 15 wherein said graph generator, said graph converter and said description generator are embodied in sequences of instructions executable in a general purpose computing system.

20. (Original) The system as recited in Claim 15 wherein said hierarchical register consolidation structure pertains to a real-time system.